What is claimed is:

1. A capacitive structure comprising a semiconducting substrate; a conductive layer; and a dielectric layer between the substrate and the conductive layer, wherein the dielectric layer is according to the formula MSi_xO_y, wherein M is a doped or undoped rare-earth element.

2. The capacitive structure of claim 1, wherein x is in the range of 0.01 to 40, and y is in the range of 0.01 to 80.

3. The capacitive structure of claim 1, wherein the element is Pr, Nd, Sm, Eu, Gd, Dy, Ho, Er, Tm, Yb, or Lu.

4. The capacitive structure of claim 3, wherein the element is gadolinium.

5. The capacitive structure of claim 4, wherein the dielectric layer is amorphous.

6. The capacitive structure of claim 3, further comprising a buffer layer between the substrate and the dielectric layer.

7. The capacitive structure of claim 6, wherein the buffer is silicon dioxide.

8. The capacitive structure of claim 6, wherein the buffer is silicon oxynitride.

9. The capacitive structure of claim 3, wherein the substrate has a substrate surface comprising a termination layer of hydrogen atoms.

10. The capacitive structure of claim 3, wherein the substrate has a substrate surface comprising a termination layer of oxygen atoms.

11. A method of producing a capacitive structure, the method comprising the steps of:

providing a semiconducting substrate having a surface;

forming over said surface, a dielectric layer according to the formula MSi_xO_y, wherein M is a doped or undoped rare-earth element; and

annealing the resulting rare-earth containing layer.

12. The method of claim 11, wherein said step of forming said dielectric layer comprises the step of exposing the substrate surface to a simultaneous or sequential flux of metalorganic or other molecules containing rare-earth atoms, silicon atoms and oxygen atoms.

13. The method of claim 12, wherein the rare-earth atoms are Pr, Nd, Sm, Eu, Gd, Dy, Ho, Er, Tm, Yb, or Lu atoms.

14. The method of claim 13, wherein the rare-earth atoms are gadolinium atoms.

15. The method of claim 13, wherein said annealing is effected in vacuum.

16. The method of claim 13, wherein said annealing is effected in an inert gas such as N_2.

17. The method of claim 13, wherein said annealing is effected in a noble gas such as A, Ne, Kr, or Xe.

18. The method of claim 13, further including the step of cleaning said surface.

19. The method of claim 13, further comprising the step of depositing a buffer layer between the substrate and the dielectric layer.

20. The method of claim 13, further comprising the step of treating the surface so to terminate with one monolayer or less of hydrogen atoms.

21. The method of claim 13, further comprising the step of treating the surface to terminate with one monolayer or less of oxygen atoms.

22. The method of claim 14, wherein the step of forming said dielectric layer further comprises the step of placing said surface in a chamber which has a partial pressure of oxygen-bearing molecules $< 10^{-7}$ Torr at a temperature of from about 800 °C to about 1000 °C.

23. The method of claim 22, wherein the chamber contains inert, non-reactive gases such as N_2, He, Ne, A, Kr, or Xe.

24. A semiconductor device comprising a capacitive structure having a semiconducting substrate; a conductive layer; and a gate dielectric between the substrate and the conductive layer, wherein the gate dielectric is according to the formula MSi_xO_y, wherein M is a doped or undoped rare-earth element.

25. The device of claim 24, wherein the device is a transistor.

26. The device of claim 25, wherein the transistor is a field effect transistor.

27. The device of claim 24, wherein x is in the range of 0.01 to 40, and y is in the range of 0.01 to 80.

28. The device of claim 24, wherein the element is Pr, Nd, Sm, Eu, Gd, Dy, Ho, Er, Tm, Yb, or Lu.

29. The device of claim 28, wherein the element is gadolinium.

30. The device of claim 29, wherein the gate dielectric is amorphous.

31. The device of claim 28, further comprising a buffer layer between the substrate

and the gate dielectric.

32. The device of claim 31, wherein the buffer is silicon dioxide.

33. The device of claim 31, wherein the buffer is silicon oxynitride.

34. The device of claim 28, wherein the substrate has a substrate surface comprising a termination layer of hydrogen atoms.

35. The device of claim 28, wherein the substrate has a substrate surface comprising a termination layer of oxygen atoms.

36. An integrated circuit having a semiconductor device fabricated thereon, including a gate dielectric of a doped or undoped rare-earth silicate.